Complete If Known Application Number 10/662,204 Filing Date September 12, 2003 First Named Inventor Nguyen et al. Art Unit 2819 Examiner Name Cho, James Hyonchol Art Unit 2819 Examiner Name Cho, James Hyonchol Complete If Known Nguyen et al. Art Unit 2819 Examiner Name Cho, James Hyonchol Art Unit Complete If Known Name of Name of Patentee or Name of Patentee or Name of Patentee or Name of Inventor Name of Inv										
Filing Date September 12, 2003 Nguyen et al. Art Unit 2819 Examiner Name Cho, James Hyonchol Examiner Name Cho, James Hyonchol Cho, Ja		DOTO-BASATIO	NI DICC		Complete If Known					
Filing Date		WALCHONG ST	DISCI	Application Number						
Pirst Named Inventor	\perp		Filing Date							
Art Unit Examiner Name Cho, James Hyonchol Cho, James Hyo	1	· [[] • · • • · • · • ·	First Named Invent	tor						
Sheet	1 7		O-1449							
Silect	Cha			Examiner Name				onchal		
U.S. PATENT DOCUMENTS	Snee	of of		2						
Document Number Publication Date Number Kind Code Appropriate Number Kind Code Appropriate Number Kind Code Appropriate Number Kind Code Appropriate Number Kind Code Number Kind Code Number Kind Code Number Number Kind Code Number				U.S. PAT	ENT			1 00003-0	127-00	<u></u>
Minuser - Kind Code		- Document 140		ublication Date						
1,194,765 03/1993 Dunlop et al. 326 87		11411001 - 1/1110	Code' N	M-DD-YYYY	Ap	plicant of Cited Document	Class	Subclass	Fili	ng Date i
Dunlop et al. 326 87	1				Ta	ylor et al.		175	AP.	propriate
S,233,843 10/1994 Sugibayashi, Tadahiko 327 541					Du	nlop et al.			+	 ,
Sp. 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1,					Ho	rowitz et al.			+	/
Systematics	 		12	2/1994	Su	gibayashi, Tadahiko			+	
System									+	
Signature Sign	}				Wa	ills				
10/1998 10/1998 10/1998 10/1998 10/1998 10/1998 10/1998 10/1999 10/1			07	/1998	00	ishi. Tsukasa			+	-+-
12/1998	-		10	/1998					+	
1.5,935,051 08/1999 Tsuchida et al. 323 315			12	/1998	No	akes et al			+	
S.949.254 09/1999 Keeth 326 87			08	/1999			+		+	
5,959,481 09/1999		5,949,254							╃—	
Class Cla		5,959,481								/
Country Code* Number Publication Date MM-DD-YYYY Applicant of Cited Document Class Subclass No		6,047,346							 	<i> </i>
6,222,354		6,163,178							 	<u> </u>
G,342,800 01/2002 Stark et al. 327 170									1	
G,618,786 09/2003 Sidiropoulos et al. 710 305		6,342,800	01/	2002					 _/	
Control Code* Onumber Publication Date Name of Patentee or Class Subclass Yes No		6,618,786			_				+	
Foreign Patent Document Foreign Patent Document Country Code ² - Number Name of Patentee or Applicant of Cited Document Kind Code ³ (If known) Publication Date MM-DD-YYYY Applicant of Cited Document Class Subclass Yes No	V	6,657,468							 /-	
FOREIGN PATENT DOCUMENTS Examiner Initials Foreign Patent Document Country Code* - Number - Kind Code* (if known) Publication Date MM-DD-YYYY Applicant of Cited Document Rep 0 463 316 A1 01/02/1992 H04L 12/40 EP 0 482 392 A2 04/29/1992 H04L 25/08 DTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS Examiner Initials Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, causlog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published Allen, Arnold O., "Probability, Statistics, and Queuing Theory with Computer Science Applications", 2nd Edition, CH 7, pp 450, 458-459 Chappell, Terri I. et al., "A 2ns Cycle, 4ns Access 512 kb CMOS ECL SRAM", IEEE International Solid State Circuits Conference, 1991, pp 50-51 Donnelly, Kevin S. et al., "A 660 MB/s Interface Megacell Portable Circuit in 0.3 µm-0.7 µm CMOS Examiner Signature Date Considered Date Da	yc	6,661,268			_				 / _	
Foreign Patent Document Publication Date Name of Patentee or Applicant of Cited Document Class Subclass Yes No							321 .	170	<u>/</u>	
Initials Country Code ² - Number Kind Code (if known) EP 0 463 316 A1 01/02/1992 H04L 12/40 EP 0 482 392 A2 04/29/1992 H04L 25/08 OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS Examiner Initials Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, causlog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published Allen, Arnold O., "Probability, Statistics, and Queuing Theory with Computer Science Applications", 2nd Edition, CH 7, pp 450, 458-459 Chappell, Terri I. et al., "A 2ns Cycle, 4ns Access 512 kb CMOS ECL SRAM", IEEE International Solid State Circuits Conference, 1991, pp 50-51 Donnelly, Kevin S. et al., "A 660 MB/s Interface Megacell Portable Circuit in 0.3 μm-0.7 μm CMOS ASIC", IEEE Journal of Solid State Circuits, 31(12):1995-2003 (1996) No μονι Τη CMOS Examiner Signature Date Considered Class Subclass Translation Yes No No Yes N	Evamines	Foreign Patent Doc	cument		LEIVE	DOCUMEN 15				
Kind Code* (if known) MM-DD-YYYY Applicant of Cited Document Class Subclass Yes No		Country Code - Nu	mber - Put	Publication Date	1	Name of Patentee or	Cla		Trans	lation
EP 0 482 392 A2 O4/29/1992 P JP 58-54412 (A) O3/3 1/1983 OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS Examiner Initials Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published Allen, Arnold O., "Probability, Statistics, and Queuing Theory with Computer Science Applications", 2nd Edition, CH 7, pp 450, 458-459 Chappell, Terri I. et al., "A 2ns Cycle, 4ns Access 512 kb CMOS ECL SRAM", IEEE International Solid State Circuits Conference, 1991, pp 50-51 Donnelly, Kevin S. et al., "A 660 MB/s Interface Megacell Portable Circuit in 0.3 µm-0.7 µm CMOS Examiner Signature Date Considered Date Considered Date Considered Date Considered Date Considered	- L-	Kind Code (if kno	U#71/	MM-DD-YYYY		Applicant of Cited Document		Subclass	Yes	No
IP 58-54412 (A) OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS Examiner Initials Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, caialog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published Allen, Arnold O., "Probability, Statistics, and Queuing Theory with Computer Science Applications", 2nd Edition, CH 7, pp 450, 458-459 Chappell, Terri I. et al., "A 2ns Cycle, 4ns Access 512 kb CMOS ECL SRAM", IEEE International Solid State Circuits Conference, 1991, pp 50-51 Donnelly, Kevin S. et al., "A 660 MB/s Interface Megacell Portable Circuit in 0.3 µm-0.7 µm CMOS Examiner Signature Date Considered Date Considered Date Considered Date Considered	-12						H041.	12/40	1	
OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS Examiner Initials Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published Allen, Arnold O., "Probability, Statistics, and Queuing Theory with Computer Science Applications", 2nd Edition, CH 7, pp 450, 458-459 Chappell, Terri I. et al., "A 2ns Cycle, 4ns Access 512 kb CMOS ECL SRAM", IEEE International Solid State Circuits Conference, 1991, pp 50-51 Donnelly, Kevin S. et al., "A 660 MB/s Interface Megacell Portable Circuit in 0.3 µm-0.7 µm CMOS ASIC", IEEE Journal of Solid State Circuits, 31(12):1995-2003 (1996) No month	- 16			29/1992						
Examiner Initials Examiner Initials Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, scrial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published Allen, Arnold O., "Probability, Statistics, and Queuing Theory with Computer Science Applications", 2nd Edition, CH 7, pp 450, 458-459 Chappell, Terri I. et al., "A 2ns Cycle, 4ns Access 512 kb CMOS ECL SRAM", IEEE International Solid State Circuits Conference, 1991, pp 50-51 Donnelly, Kevin S. et al., "A 660 MB/s Interface Megacell Portable Circuit in 0.3 µm-0.7 µm CMOS ASIC", IEEE Journal of Solid State Circuits, 31(12):1995-2003 (1996) Date Considered Considered	_ <i>F</i>						GOSEL		_	Fall
Initials Initia	Evenine	OT	HER PRIOR	ART - NON PA	TENT	LITERATURE DOCUM				
Allen, Arnold O., "Probability. Statistics, and Queuing Theory with Computer Science Applications", 2nd Edition, CH 7, pp 450, 458-459 Chappell, Terri I. et al., "A 2ns Cycle, 4ns Access 512 kb CMOS ECL SRAM", IEEE International Solid State Circuits Conference, 1991, pp 50-51 Donnelly, Kevin S. et al., "A 660 MB/s Interface Megacell Portable Circuit in 0.3 µm-0.7 µm CMOS Examiner Signature Date Considered Date Considered Date Considered		include name of the	author fin ("A PI"	'Allerrency .:				m (book mae	azine icu	mel
2nd Edition, CH 7, pp 450, 458-459 Chappell, Terri I. et al., "A 2ns Cycle, 4ns Access 512 kb CMOS ECL SRAM", IEEE International Solid State Circuits Conference, 1991, pp 50-51 Donnelly, Kevin S. et al., "A 660 MB/s Interface Megacell Portable Circuit in 0.3 μm-0.7 μm CMOS ASIC", IEEE Journal of Solid State Circuits, 31(12):1995-2003 (1996) Date Considered Date Considered		Allen Arnold O	"Drobabilit	c.), date, page(s), v	olume-	issue number(s), publisher, cit	y and/or cour	ntry where pul	lished	*******
Chappell, Terri I. et al., "A 2ns Cycle, 4ns Access 512 kb CMOS ECL SRAM", IEEE International Solid State Circuits Conference, 1991, pp 50-51 Donnelly, Kevin S. et al., "A 660 MB/s Interface Megacell Portable Circuit in 0.3 µm-0.7 µm CMOS Examiner Signature Date Considered Considered Syl-5		***************************************	LIVUAUIII	A" STATISTICS &	ua C)	neuing Theory with C	omputer :	Science A	plicati	ons",
ASIC", IEEE Journal of Solid State Circuits, 31(12):1995-2003 (1996) No month Signature Date Considered 8/1-5	L	Channell Terri I	et al "A 2"	0-439			·			
ASIC", IEEE Journal of Solid State Circuits, 31(12):1995-2003 (1996) No month Signature Date Considered 8/1-5	or	Solid State Circuit	its Conform	is Cycle, 4hs	Acce:	ss > 12 kb CMOS ECL	SRAM"	, IEEE Inte	rnatio	nal
ASIC", IEEE Journal of Solid State Circuits, 31(12):1995-2003 (1996) No month Signature Date Considered 8/1-5	1	Donnelly Kevin	S et al "A	660 MD/s T	U-51	100 MONA	<u>r</u>			_ [
Examiner Signature Date Considered 8/2/-5	K						ircuit in O	.3 μm-0.7	μm Cλ	10S
Signature Ch. Date Considered 8/2/-5	Examiner	7.223.001	oj 5011a	Siale Circuit	5, 31(12):1995-2003 (1996) /\	10 mor	174		
Considered		1	mes 1	~A_			01-	101		一
EXAMINER: Initial if my		D. Initial is				Considered	0 1'2	1-3	_	1

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). For Japanese patent documents, the indication of the year of the reign of the Emperor must

precede the serial number of the patent document. Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. Applicant is to place a check mark here if English language Translation is attached. Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

INT	ORMATI	ON DISCL	OOIME	Complete If Known					
1 1111			OSUKE	Application Number	10/662,204				
	CH	ATION		Filing Date	September 12, 2003				
				First Named Inventor	Nguyen et al.				
PTO-1449				Art Unit	2819				
Sheet	T			Examiner Name	Cho, James Hyonchol				
	2	of	2	Attorney Docket Number	60200 0127 115				
I G	International Solid State Circuits Conference, pp. 148-149 (1996) Schumacher, Hans-Jürgen et al., "CMOS Subnanosecond True-ECL Output Buffer", IEEE Journal of Solid-State Circuits", 25(1):150-154 (1990) Sidiropoulos, Stefanos et al., "A 700-Mb/s/pin CMOS Signaling Interface Using Current Integrating Receivers", IEEE Journal of Solid-State Circuits", 32(5):681-690 (1997) Yang, Tsen-Shau et al., "A 4-ns 4Kx1-bit Two-Port BiCMOS SRAM", IEEE Journal of D-State Circuits", 23:(5):1030-1040 (1988) EIA/JDEC, JC-42.3 Committee on RAM Memories, Minutes of Meeting 63, July 21, 1992, Denver, Crystal City, VA.								

Examiner Date Signature Considered

^{*}EXAMINER: Initial preference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. Applicant is to place a check mark here if English language Translation is attached. Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.